What is claimed is:

1. A method of manufacturing an integrated circuit package, comprising:

installing a carrier onto an upper surface of a substrate, wherein said carrier defines a cavity;

attaching a semiconductor die to said upper surface of said substrate within said cavity of said carrier;

aligning an assembly over said semiconductor die, wherein said assembly comprises a heat sink and a thermally conductive element;

resting said assembly on said carrier such that said thermally conductive element does not directly contact said semiconductor die; and

encapsulating said cavity to form a prepackage such that a portion of said heat sink is exposed to the surroundings of said package.

2. The method of claim 1, wherein said assembly is rested on said carrier such that said thermally conductive element and said semiconductor die are separated by a distance of about five (5) mils or less.

3. The method of claim 1, wherein said attaching said semiconductor die to said upper surface of said substrate is by a direct chip attachment.

4. The method of claim 1, further comprising singulating said prepackage to form said package, wherein a top portion and a side portion of said heat sink are exposed to the surroundings of said package.

5. A method of manufacturing an integrated circuit package, comprising:

installing a carrier onto a substrate;

attaching a semiconductor die to said substrate;

aligning an assembly over said semiconductor die, wherein said assembly comprises a heat sink and a thermally conductive element;

resting said assembly on said carrier such that said thermally conductive element does not directly contact said semiconductor die; and

encapsulating said thermally conductive element and said heat sink such that a portion of said heat sink is exposed to the surroundings of said package.